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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,309	PACHA ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/2/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-28,31-37 and 39-50* is/are rejected.

7)☒ Claim(s) *29,30 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 6/7/2004. Claims 24-50 are under examination.

Claim Objections

1. Claim 1 is objected to because of the following informalities: the recitation of "if" in line 5 is not a positive recitation. It is suggested to change "if" to --when--. Appropriate correction is required.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of "third power switch transistor is a p MOS field effect transistor" of claim 32, "a control unit" of claim 38 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

3. The drawings are objected to because figure 6 shows transistor 602 as an nMOS field effect transistor instead of p MOS field effect transistor as described in page 30, line 21 and claimed in claim 32.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 26, 31-32, 37, 41 and 43-50 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 26, the recitation of "the first power switch transistor is common power switch transistor provided for the flip flop and for at least one additional flip flop" is indefinite because it is misdescriptive of the present invention. Figure 3 shows the power switch transistor (303) couples the additional flip flop (309, 310, 315, 316) to Vss. The flip flop (301) is coupled directly to VDDL and VSS. Therefore, the first power switch transistor is not a common power switch transistor to the flip flop and the additional flip flop as recited. Correction is required.

In claim 31, the recitation of "a third power switch transistor" lacks proper antecedent basis because there is no second power switch transistor recited in claims 24.

In claim 37, the recitation of "fifth value" lacks proper antecedent basis because there is no fourth value defined in claims 24, 33 and 36.

In claim 41, the recitation of "sixth value" lacks proper antecedent basis because there is no fifth value defined in claims 24 and 39.

In claims 43 and 44, the recitation of "the test transistors" lacks proper antecedent basis.

In claim 47, the recitation of "seventh value" lacks proper antecedent basis because there is no fourth value defined in claims 24, 33 and 34.

In claim 48, the recitation of "seventh value" lacks proper antecedent basis because there is no fourth value defined in claims 24, 33, 35, 36 and 37.

In claim 45, the recitation of "seventh value" lacks proper antecedent basis because there is no fourth value defined in claim 24.

Claims 32, 42, 46 and 49-50 are indefinite because of the technical deficiencies of claims 31, 41 and 45.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 24-25 and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiguchi et al. (USP 5,583,457). Figure 29 of Horiguchi et al. shows a circuit arrangement comprising a flip flop (LH) having a plurality of storage transistors with a threshold voltage of a

first value (high threshold), a first power switch transistor (MP1, MN1) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (CK, CKB) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (MP2, MN2), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage) as called for in claim 24.

Regarding claim 25, the flip flop (LH) has two inverters.

Regarding claim 27, since the storage and the first power switching transistors have a higher threshold voltage, the thickness of the gate insulating layer of the storage transistors and the first power switch transistor is greater than the thickness of the gate insulating layer of the switching transistors.

Regarding claim 28, since the storage and the first power switching transistors have a higher threshold voltage, the channel width of the storage transistors and the first power switch transistor is less than the thickness of the gate insulating layer of the switching transistors.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 24-25, 27-28, 33-37, 45-46 and 49-50 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuzaki et al. (6,500,715). Figure 14 of Matsuzaki et al. shows a circuit

arrangement comprising a flip flop (LH1 details shown in figure 8) having a plurality of storage transistors with a threshold voltage of a first value (high threshold), a first power switch transistor (MN1) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (CS) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (TP1-TP3, TN1-TN3), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage) as called for in claim 24.

Regarding claim 25, the flip flop (LH1) has two inverters.

Regarding claim 27, since the storage and the first power switching transistors have a higher threshold voltage, the thickness of the gate insulating layer of the storage transistors and the first power switch transistor is greater than the thickness of the gate insulating layer of the switching transistors.

Regarding claim 28, since the storage and the first power switching transistors have a higher threshold voltage, the channel width of the storage transistors and the first power switch transistor is less than the thickness of the gate insulating layer of the switching transistors.

Regarding claims 24 and 33, figure 45 of Masuzaki et al. shows a circuit arrangement comprising a flip flop (LH2 details shown in figure 8) having a plurality of storage transistors

with a threshold voltage of a first value (high threshold), a first power switch transistor (MP1) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (CS) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (IV1), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage) as called for in claim 24.

Regarding claim 33, figure 45 shows a pulse generator (NA1) that generates a flip flop input signal from an input signal (Ai, Aj) and from a clock signal (ϕ) and is coupled to the first power switch transistor (MP1) and to the switching transistors (IV1).

Regarding claims 34 and 37, figure 45 of shows the pulse generator (NA1) having transistors with low threshold voltages.

Regarding claims 35-36, figure 45 shows the subcircuit NA1 generates at least one flip flop input signal from at least one input signal Ai with a predetermined logic operation (nand logic operation).

Regarding claims 47-48, figure 45 of Matsuzaki et al. shows the protection transistors MP5, MN5 having high threshold voltage.

Regarding claims 45 and 50, figure 14 of Matsuzaki et al. shows the protection transistors MP4, MN4 having high threshold voltage.

Regarding claim 46, since the protection transistors have a higher threshold voltage, the thickness of the gate insulating layer of the protection are greater than the thickness of the gate insulating layer of the switching transistors.

Regarding claim 49, in a first operating state, power switch MN1 switches off power supply to the switching transistors, the same control signal CS also electrically decouple the flip flop form the switching transistors, in a second operating state, the power switch MN1 connecting the power supply to the switching transistors, the protection circuit electrically couples the flip flop to the switching transistors.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (USP 5,583,457) in view of Sani et al. (USP 6,794,914).

Figure 29 of Horiguchi et al. shows a circuit arrangement comprising a flip flop (LH) having a plurality of storage transistors with a threshold voltage of a first value (high threshold), a first power switch transistor (MP1, MN1) having a second threshold voltage (high threshold),

wherein an application of a predetermined electrical potential (CK, CKB) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (MP2, MN2), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage). Horiguchi et al. does not disclose a test circuit coupled to the flip flop for testing the functionality of the flip flop as called for in claim 39. Sani et al. shows a flip flop having a test circuit (310 of figure 3) to test and to enhance the reliability of the flip flop. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to include Sani et al.'s test circuit in the circuit arrangement of Horiguchi et al. for purpose of enhancing the reliability of the flip flop.

Regarding claim 40, the combination of Horiguchi et al. and Sani et al. show the test circuit comprising a test input signal (Sin), output components (output of the flip flop) that reads a test output signal of the flip flop.

Regarding claim 41, the combination of Horiguchi et al. and Sani et al. show the test circuit comprising a plurality of transistors (322, 324) having a high threshold voltage.

Regarding claim 42, since test transistors have a higher threshold voltage than the threshold voltage of the switching transistors, the thickness of the gate insulating layer of the test transistors are greater than the thickness of the gate insulating layer of the switching transistors.

11. Claims 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. (USP 6,500,715) in view of Sani et al. (USP 6,794,914).

Figure 14 of Matsuzaki et al. shows a circuit arrangement comprising a flip flop (LH1 details shown in figure 8) having a plurality of storage transistors with a threshold voltage of a first value (high threshold), a first power switch transistor (MN1) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (CS) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (TP1-TP3, TN1-TN3), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage). Matsuzaki et al. does not disclose a test circuit coupled to the flip flop for testing the functionality of the flip flop as called for in claim 39. Sani et al. shows a flip flop having a test circuit (310 of figure 3) to test and to enhance the reliability of the flip flop. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to include Sani et al.'s test circuit in the circuit arrangement of Matsuzaki et al. for purpose of enhancing the reliability of the flip flop.

Regarding claim 40, the combination of Matsuzaki et al. and Sani et al. show the test circuit comprising a test input signal (Sin), output components (output of the flip flop) that reads a test output signal of the flip flop.

Regarding claim 41, the combination of Matsuzaki et al. and Sani et al. show the test circuit comprising a plurality of transistors (322, 324) having a high threshold voltage.

Regarding claim 42, since test transistors have a higher threshold voltage than the threshold voltage of the switching transistors, the thickness of the gate insulating layer of the test transistors are greater than the thickness of the gate insulating layer of the switching transistors.

12. Claims 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. (USP 6,500,715) in view of Sani et al. (USP 6,794,914).

Figure 45 of Masuzaki et al. shows a circuit arrangement comprising a flip flop (LH1 details shown in figure 8) having a plurality of storage transistors with a threshold voltage of a first value (high threshold), a first power switch transistor (MP1) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (CS) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (IV1), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage). Matsuzaki et al. does not disclose test transistors, coupled to the flip

flop, having a gate thickness greater than the gate thickness of the transistors of the pulse generator as called for in claims 43 and 44. Sani et al. shows a flip flop having a test circuit (310 of figure 3) to test and to enhance the reliability of the flip flop. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to include Sani et al.'s test circuit in the circuit arrangement of Matsuzaki et al. for purpose of enhancing the reliability of the flip flop. Further, since test transistors have a higher threshold voltage than the threshold voltage of the pulse generator's transistors, the thickness of the gate insulating layer of the test transistors are greater than the thickness of the gate insulating layer of the pulse generator's transistors

Allowable Subject Matter

13. Claims 26 and 31-32 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

14. Claims 29-30 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

11/08/2004